J. Microelectron. Manuf. **3**, 20030105 (2020)
doi: 10.33079/jomm.20030105

# A Device Design for 5 nm Logic FinFET Technology

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**Abstract:** With the continuous scaling in conventional CMOS technologies, the planar MOSFET device is limited by the severe short-channel-effect (SCE), Multi-gate FETs (MuG-FET) such as FinFETs and Nanowire, Nanosheet devices have emerged as the most promising candidates to extend the CMOS scaling beyond sub-22 nm node. The multi-gate structure has better short channel behaviors due to enhanced control from the multiple gates. Due to the relatively more mature process and rich learning of the device physics, the FinFET is still extended to 5 nm technology node. In this paper, we proposed a 5 nm FINFET device, which is based on typical 5 nm logic design rules. To achieve the challenging device performance target, which is around 15% speed gain or 25% power reduction against the 7 nm device, we have performed an optimization on the process parameters and iterate through device simulation with the consideration of current process capability. Based on our preferred device architecture, we provide our brief process flow, key dimensions, and simulated device DC/AC performance, like Vt, Idsat, SS, DIBL and parasitic parameters. As a part of the final evaluation, RO simulation result has been checked, which demonstrates that the Performance Per Area (PPA) is close to industry reference 5 nm performance.

**Keywords:** 5nm FinFET, brief process flow, key dimensions, simulated device DC/AC performance, RO PPA performance.

## 1. Introduction

As MOSFET scales down, the conventional planar transistor architectures have already reached the fundamental material and process technology limits. Besides, as the size decreases, the device will suffer from the short channel effects (SCE), which result in the severe leakage problem and mobility degradation, and hence the effective drive current will drop. The threshold voltage (Vt) will also roll-off. Thus, a high channel doping to control the leakage current is required. However, it has major disadvantages of lower carrier mobility, high tunneling effect, degradation in subthreshold performance, and larger parasitic capacitance.

Therefore, the development of small devices with high performance becomes more challenging. Innovative three-dimensional structures such as double-, triple-, fin-typed, nanosheet, and nanowire field-effect transistors (FET) have been of great interests. Fin-typed FET (FinFET) is one of the most promising device structures to address short-channel effects and leakage issues in the deeply nano-scale transistor. FinFET structure mitigates these problems at low channel doping conditions, which also minimizes variations of the Vt, reduces subthreshold leakage current, keeps high carrier mobility, and enhances the drive current. Thus the FinFET structure can be scaled down to 22 nm and beyond.

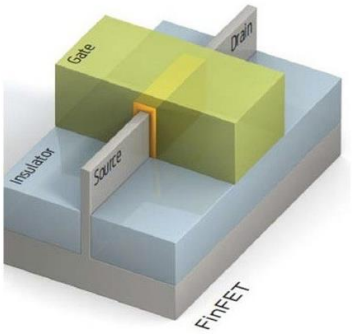


Figure 1. Schematic of FINFET Structure.

In this paper, we have developed a 5 nm FINFET structure with TCAD simulation support. In

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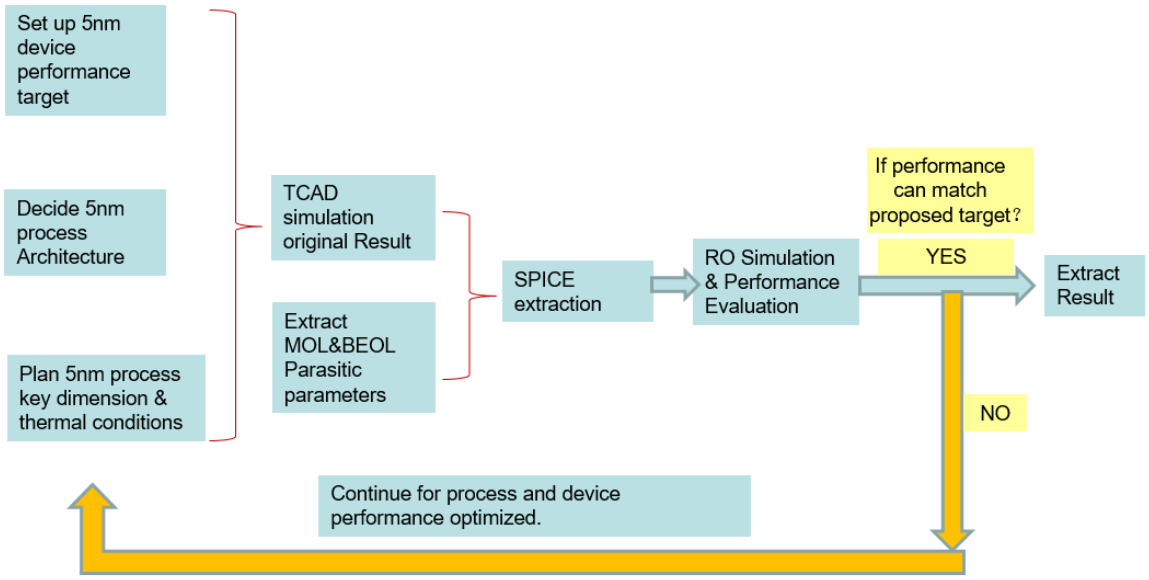



Figure 2. 5 nm device development procedure.

details, we propose our development procedure, introduce our brief process flow, present key dimensions and simulated device performance.

## 2. Simulation Approach

### 2.1. Device Development Procedure

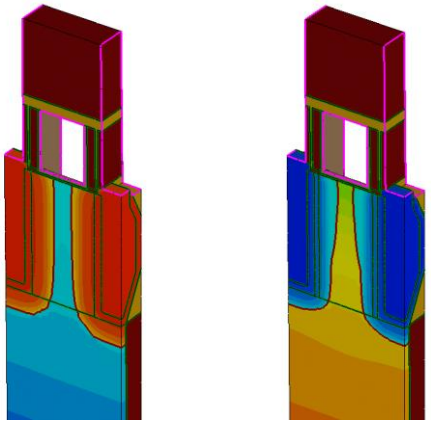
Firstly, we introduce our 5 nm development procedure shown in Figure 2, as follows.

In the beginning, we set up our device targets through material path-finding study, and then determine the architecture and process conditions. We perform the TCAD simulation with these conditions ready and get the initial result. Next combine with Middle-Of-the-Line (MOL) & Back-End-Of-The-Line (BEOL) extracted parasitic parameters, we extract the SPICE model parameters, and take the result into Ring Oscillator (RO) simulation, if the Performance Per Area (PPA) can meet our initial target, then we extract our device data and curves as a result; if not, then as a learning circle, we will continue to optimize our simulation conditions.

### 2.2. Device structure

Figure 3 illustrates the device architecture of the simulated FinFET and cross-section view of the device doping profile.

In this simulation, a Fin pitch of 24 nm, a Poly pitch of 50 nm, and a total gate length (LG) of 19 nm have been adopted. We set the top fin-width ($T_{fin}$) = 5 nm and the fin-height (FH) equal to 50-55 nm as a standard device; ($SiO_2$+$HfO_2$) were considered as the gate oxide and (low K+ high K $Si_3N_4$) as spacer material. Fixed total spacer length (LSP) of 5 nm was used. The doping concentrations were Phosphorus 1.0E21 for NFET and Boron 1.2E21 for PFET respectively in the source/drain (S/D) region. Around 15 nm contact (CT) dimension was applied. The key dimension of different parameters for the simulated device is listed in Table 1.



(a) (b)

Figure 3. (a) NFET, (b) PFET.

### 2.3. Device structure

The brief process flow used in our 5 nm FinFET device simulation was shown in Figures 4.1 and 4.2. First, we define the fin profile, and the critical dimension of fin width has been shown in Table I. Followed by STI deposition, and then the poly gate formation, in which the gate region is wrapped

Table 1. Device parameters used in the simulation.

| Process Stage | Process Description | Unit | Size |
|---|---|---|---|
| Gate Length | Gate Length | nm | 19 |
| Fin pitch | Fin Pitch | nm | 24 |
| Poly Pitch | Poly Pitch | nm | 50 |
| TFin | Fin TOP CD | nm | 5 |
| Hfin | Fin height | nm | 50-55 |
| EOT | Thfo2 thickness | A | 12 |
| Tspacer | Low K + high K spacer thickness | nm | 5 |
| SD Epi | SD Epi Trench Depth | nm | 50-55 |
| | Layer doping: Phosphorus(NMOS) | | 1.0E+21 |
| | Layer doping: Ge/Boron (PMOS) | | 50%/1.2E21 |
| CT | CT size | nm | ~15 |

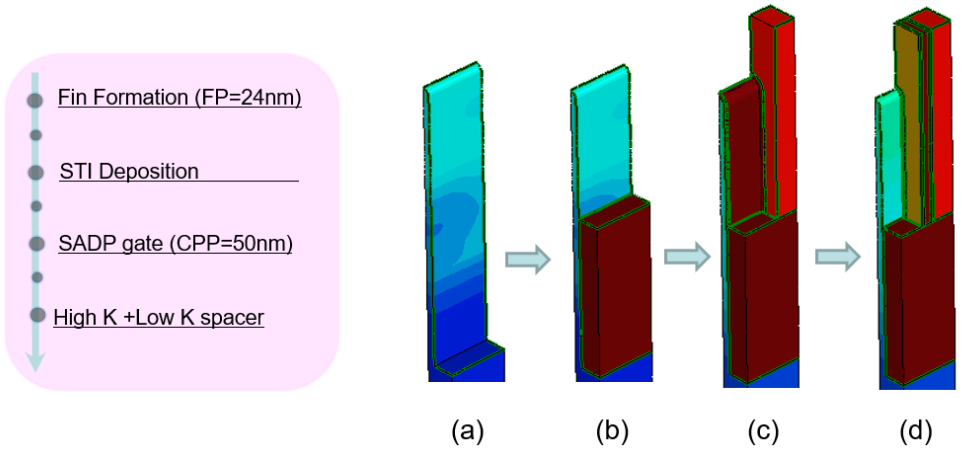



Figure 4.1. General process flow of a FINFET device simulation with process steps (a) through (d).

around the three sides of the fin channel. The gate oxide is formed under the gate. By extending gate control to three sides of the fin, it will allow the relatively shorter gate length. Next, S/D offset spacers and spacers are formed along the sidewalls of the gate and fin. The sidewall spacers on the fins are subsequently removed to expose the fin to grow raised source and drain using selective epitaxy.

Source and drain extensions are formed by epitaxy, the raised source and drain structure help to reduce the parasitic resistance associated with thin fins. Next, ILD film deposition and planarization, and then the gate dielectric is grown and poly gate is replaced by metal gate. Then, contact connection has been defined. Finally, before the Sentaurus S-device simulation, we should do structure reflect (To save simulation time, we just do half side structure simulation in the S-Process).

## 2.4. Simulation Result

In this section, we present our simulated device DC/AC performance in Table 2, which indicates that the Drain Induced Barrier Lowering (DIBL) is around ~25 mV and Subthreshold Slope (SS) is ~65-70 mV/decade, which is comparable with published

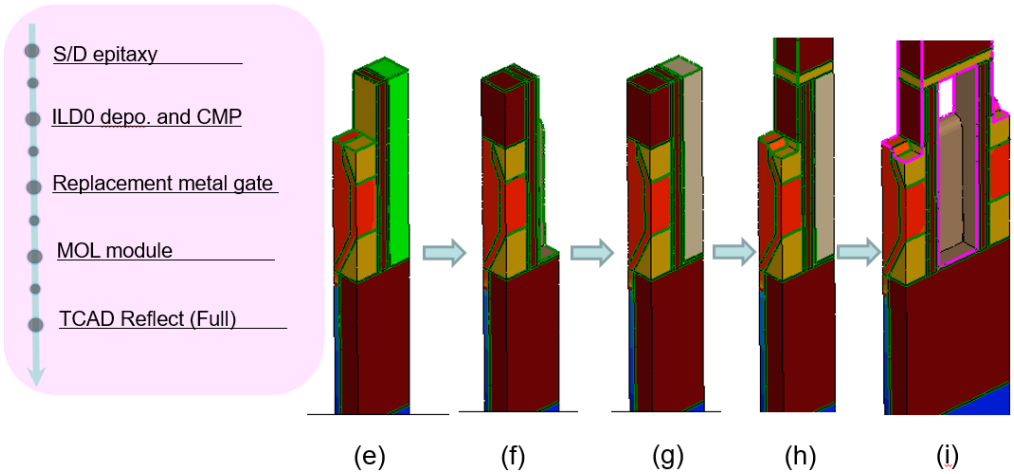



Figure 4.2. General process flow of a FINFET device simulation with process steps (e) through (i).

Table 2. The simulated device DC/AC performance result.

| | | | NMOS | PMOS |
|---|---|---|---|---|
| DC Performance | Vtlin | V | 0.163 | 0.145 |
| | Vtsat | V | 0.137 | 0.124 |
| | DIBL | V | 0.026 | 0.021 |
| | Idsat | uA/fin | 76.69 | 84.73 |
| | Ioff | nA/fin | 0.95 | 1.1 |
| | SSSat | mV/dec | 70.17 | 64.69 |
| | Ieff Ioff | uA/fin | 42.84 | 43.94 |
| | | | | |
| AC Performance | Cgd0 | fF/Fin | 0.0205 | 0.0155 |
| | Cgd | fF/Fin | 0.0383 | 0.0389 |
| | Cgg0 | fF/Fin | 0.0416 | 0.0318 |
| | Cgg | fF/Fin | 0.0767 | 0.0781 |
| | Rext | ohm/Fin | 1031 | 1257 |
| | Rchannel | ohm/Fin | 1298 | 1529 |

reference performance and demonstrate that our short channel effect has been controlled well.

The parasitic parameters, like Cgd0 is around 0.0205 fF/Fin and 0.0155 fF/Fin for NFET and PFET respectively; Both Rext and Rchannel are also acceptable, NFET has around ~1031ohm/Fin Rext and ~1298ohm/Fin Rchannel, PFET has around ~1257ohm/Fin Rext and ~1529ohm/Fin Rchannel, further improvement is ongoing.

Figure 5 and Figure 6 show the IdVd, IdVg, Cgg, Cgd curves for the NFET and PFET, respectively.

Finally, to have a comprehensive understanding, we make the Ring Oscillator (RO) simulation. In Figure 7, it seems our 5 nm RO PPA performance is close to industry reference 5 nm performance. (Industry reference is published with 35% speed gain and 65% power reduction from 14 nm to 7 nm and 14.5% speed gain and 23.5% power reduction from 7 nm to 5 nm, respectively).

## 4. Conclusion

In this paper, we have performed a simulation to study a typical 5 nm FinFET device structure and performance. The result indicates that our device performance is comparable with published reference performance and the short channel effect is controlled well; our ring oscillator simulation demonstrates that the PPA is also close to industry reference 5 nm performance. We believe that the FinFET device still has the ability to extend to 5 nm technology node with continued performance gain.

## Acknowledgments

The authors would like to thank the management team and all our team members in Shanghai ICRD center.

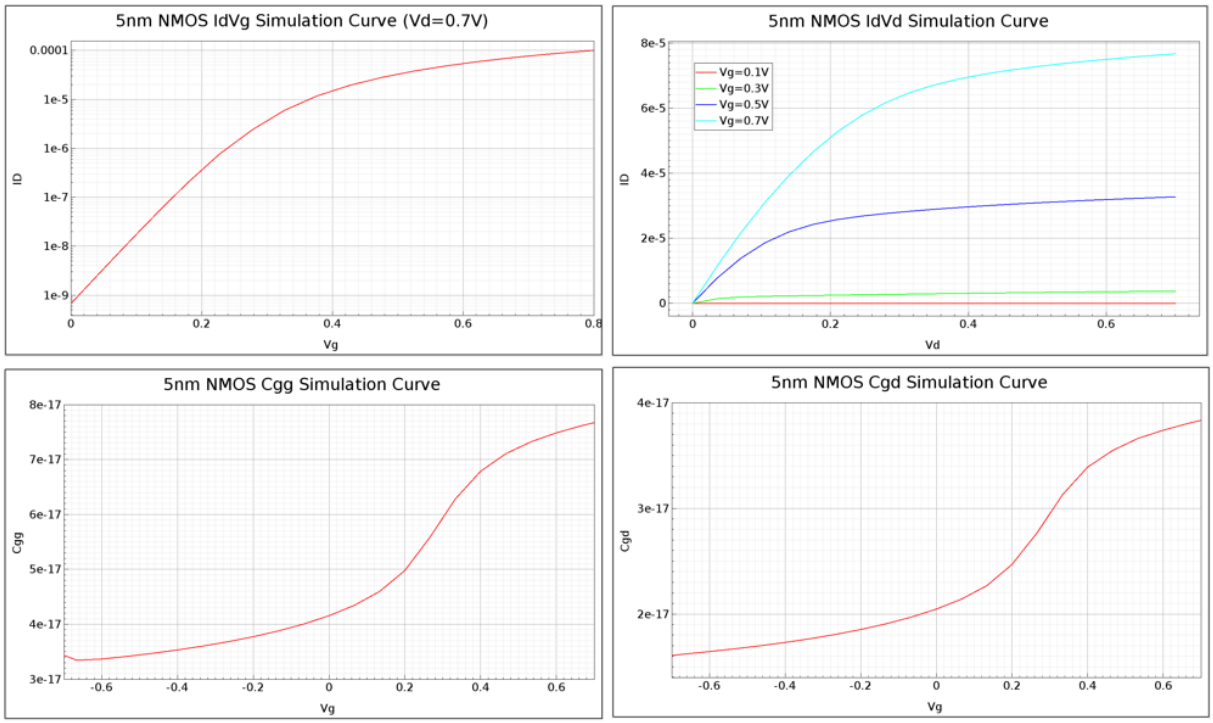



Figure 5. Characteristic curves for the NFET Device from simulation.

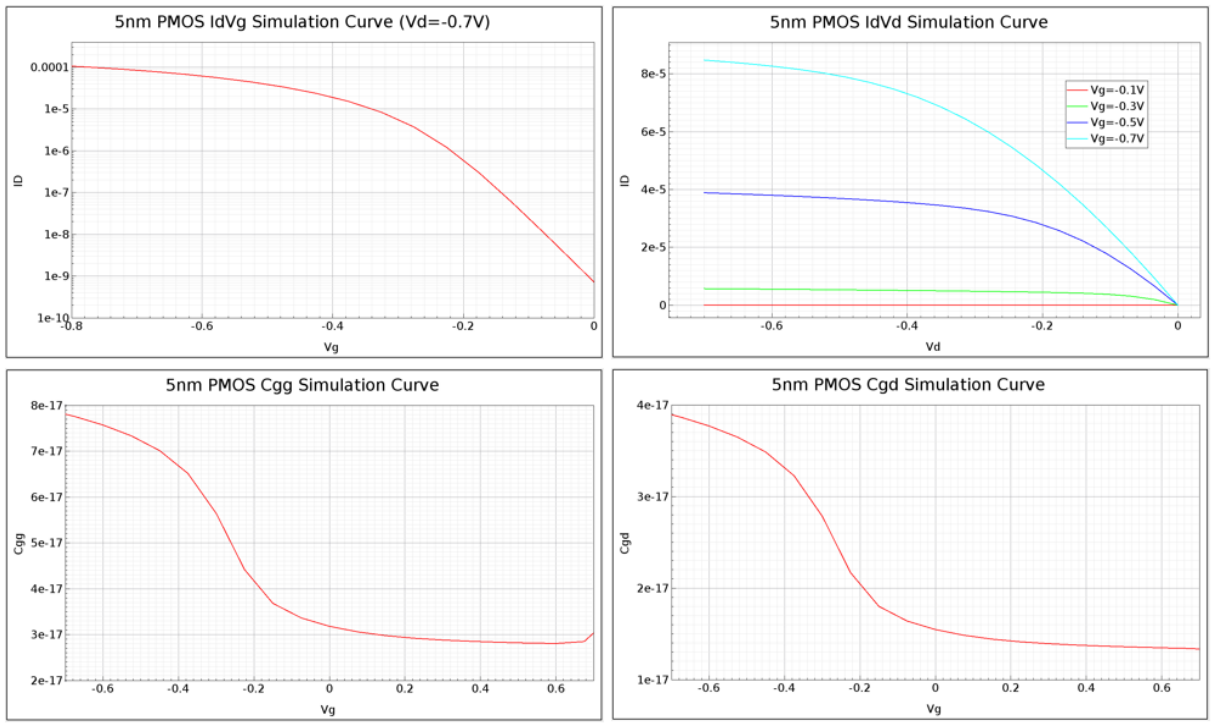



Figure 6. Characteristic curves for the PFET Device from simulation.

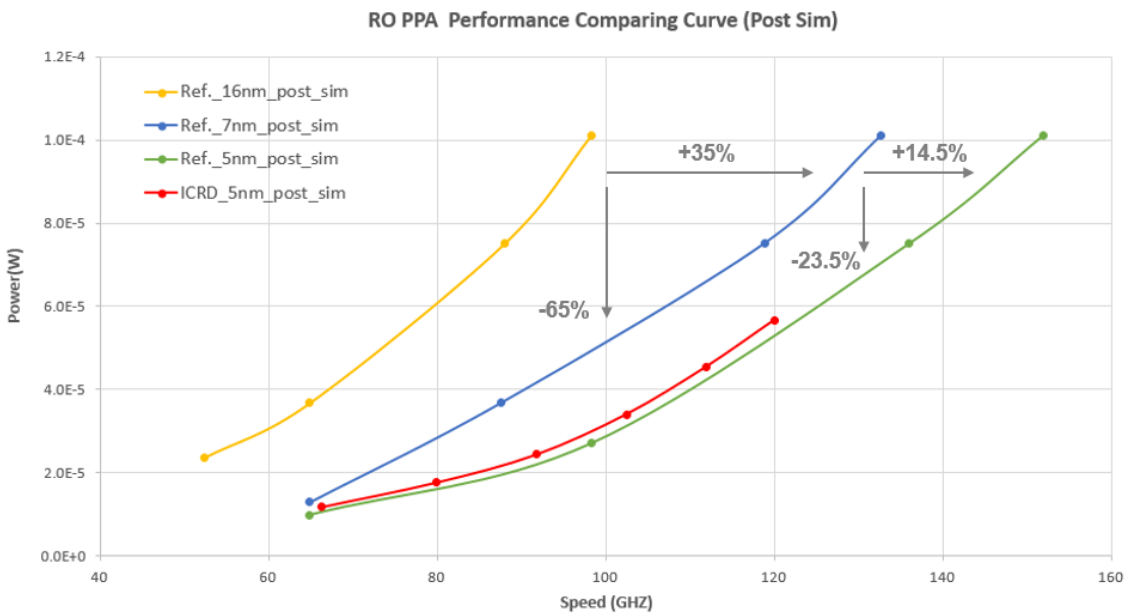



Figure 7. RO PPA performance comparison.

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